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EXAMINER
WALTER, CRAIG E

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2188	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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Office Action Summary	Application No.	Applicant(s)	
	10/665,976	BARRY ET AL.	
	Examiner	**Art Unit**	
	Craig E. Walter	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 September 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

1. Claims 1-53 are pending in the Application.

Claims 1, 7,13, 18, 29, 34, 39, and 47 are amended.

Claims 1-53 are rejected.

Response to Amendment

2. Applicant's amendments and arguments filed on 10 September 2007 in response to the office action mailed on 8 May 2007 have been fully considered, but are they are not persuasive. Therefore, the rejections are maintained, and restated below, with changes as needed to address the amendments.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-3,5, 7, 8, 10, 11, 13, 14, 16, 18, 19, 21, 22, 24-26, 39, 40, 42-44, 46-49, 52 and 53 are rejected under 35 U.S.C. 102(e) as being anticipated by

Makphaibulchoke et al. (US PG Publication 2003/0014616 A1), hereinafter Makphaibulchoke.

As for claims 1,2, 7,13, 18, 47 and 48, Makphaibulchoke teaches a method (and computer program product) comprising:

maintaining a memory management table that includes one or more entries, each entry defining a location of a portion of data stored within a memory system (paragraphs 0019 and 0027, an ACPI table is used to store data structures; pointers are used to reference locations of the data structures);

from at least two types of endian conversion, including a first type to convert data to a first endian format, and a second type to convert data to the first endian format, determining a type (data structures are stored in ACPI tables in little-endian format (in the preferred embodiment). Makphaibulchoke teaches converting the data structures in the tables from little to big-endian format. This conversion from little to big is either accomplished via byte-swapping, or bit reversal (two types of conversion to convert to a single endian format – paragraph 0019, all lines. More specifically, Fig. 5 elements 540 and 545 illustrate byte-swapping and bit reversal modules respectively. Paragraph 0024, all lines teaches illustrates how reversing the order of the bytes can produce the endian conversion. Alternately, paragraphs 0025 and 0031, all lines illustrates how this same conversion can be accomplished through reversal via shifting the bits); and

writing an entry to a memory management table specifying one of the at least two types of endian conversion based on the determining (paragraphs 0024 and 0025, all lines disclose that the conversion rearranges the data structures stored in the ACPI table. In other words, each entry in the table is converted either via bit reversal or byte swapping, hence what's written in the table is contingent upon the type of conversion that took place). More specifically, Makphaibulchoke clearly discloses multiple ACPI tables (preferred embodiment describes ten), which include multiple data structures containing data stored in little endian format (paragraph 0024, lines 15-41). These data are converted to a first endian type through one of two types of endian conversion (i.e. byte-swapping or bit-reversal) – paragraph 0024, line 35 through paragraph 0025, final line. Referring again to Fig. 6 and paragraph 0025, all lines, the data is either byte-swapped or bit-reversed based exclusively on information contained within these ACPI tables (both the data structures themselves, and their respective headers within the ACPI tables). The size of the data (evaluated at step 650), and the status of the bit field (evaluated at step 630) indicate/specify to the system what type of conversion to be performed. The information stored within these tables may be broadly construed as a "field" as recited by Applicant, since it is well known to a skilled artisan that "fields" define entries to tables. Note the conversion results in writing the converted data structure to the data which "specifies" the type of conversions that were previously determined (i.e.

the converted data is now either byte-swapped or bit reversed), therefore the format of the data itself written specify what type of conversion occurred.

As for claim 24, Makphaibulchoke teaches a memory management table residing in computer memory comprising:

one or more table entries, with each table entry having a first field for defining the location of a portion of data stored within a memory system and a second field for defining a type determined from at least two types of endian conversion (paragraphs 0024-0025, all lines – the bit field is a single bit which specifies in byte swapping or bit reversal is appropriate for the data structure. Additionally note in paragraph 0027, all lines – pointers are used to reference locations of the data structures), including a first type to convert data to a first endian format and a second type to convert data to the first endian format (as per the rationale in the rejection claim 1, *supra*).

As for claims 39 and 43, Makphaibulchoke teaches a method (and product) comprising:

accessing a table entry of a memory management table, wherein the table entry is associated with a portion of data stored within a memory system and includes a conversion-type indicator (paragraphs 0024-0025, all lines – the bit field is a single bit which specifies in byte swapping or bit reversal is appropriate for the data structure); and

from at least two types of endian conversion, including a first type to convert data to a first endian format and a second type to convert data to the first

endian format, determining a type based on the conversion-type indicator (as discussed in the rejection of claim 1 presented *supra*).

As for claims 5, 10, 16, 21, 25, 42 and 46, Makphaibulchoke teaches the entry as including a single bit for specifying one of two types of endian conversion (paragraphs 0024-0025, all lines – the bit field is a single bit which specifies in byte swapping or bit reversal is appropriate for the data structure).

As for claims 3, 8, 14, 19, 26, 40, 44 and 49, Makphaibulchoke discloses the at least two types of endian conversion as including a data coherent conversion type (paragraph 0024, Makphaibulchoke 's byte-swapping method is akin to Applicant's data coherent conversion).

As for claims 11 and 22, Makphaibulchoke teaches the portion of the data as being stored at a physical memory address within the memory system (the data structures are physically stored in the ACPI table which is stored on a memory – please refer to Fig. 5).

As for claims 52 and 53, Makphaibulchoke teaches converting either from big-little or little-bit in paragraph 0019, all lines).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 6, 12, 17, 23, 28-30, 32-35, 37 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Makphaibulchoke (US PG Publication 2003/0014616 A1) as applied to claims 1, 7, 13, 22, 24, 29 and 34 above, and in further view of Lasserre et al. (US PG Publication 2002/0069339 A1), hereinafter Lasserre.

As for claims 29 and 34, Makphaibulchoke teaches a system (and architecture) comprising:

a first processor for processing data in a first endian format (paragraph 0024, all lines and Fig. 5, element 505 – the CPU is capable of processing either big or little endian formatted data);

an endian converter for converting portions of data from the first endian format to the second endian format (Fig. 5, element 540 is a converter for byte-swapping data to complete the endian conversion); and

a memory management table including one or more entries, with each entry defining a location for a portion of data stored within a memory system to be converted from the first endian format to the second endian format, and specifying a type determined from at least two types of endian conversion, including a first type to convert data from the first endian format to the second endian format and a second type to convert data from the first endian format to the second endian format (as per the rationale in the rejection of claim 1, *supra*). More specifically, Makphaibulchoke clearly discloses multiple ACPI tables (preferred embodiment describes ten), which include multiple data structures containing data stored in little endian format (paragraph 0024, lines 15-41). These data are converted to a first endian type through one of two

types of endian conversion (i.e. byte-swapping or bit-reversal) – paragraph 0024, line 35 through paragraph 0025, final line. Referring again to Fig. 6 and paragraph 0025, all lines, the data is either byte-swapped or bit-reversed based exclusively on information contained within these ACPI tables (both the data structures themselves, and their respective headers within the ACPI tables). The size of the data (evaluated at step 650), and the status of the bit field (evaluated at step 630) indicate/specify to the system what type of conversion to be performed. The information stored within these tables may be broadly construed as a "field" as recited by Applicant, since it is well known to a skilled artisan that "fields" define entries to tables. Note the conversion results in writing the converted data structure to the data which "specifies" the type of conversions that were previously determined (i.e. the converted data is now either byte-swapped or bit reversed), therefore the format of the data itself written specify what type of conversion occurred.

Despite these teachings Makphaibulchoke fails to teach the remaining limitations of these claims.

Lasserre does in fact teach the remaining limitations, including:

a networking device (Fig. 8 illustrates the system as being implemented on a wireless networking device – paragraph 0083, all lines), including:

a second processor for processing data in a second endian format (Fig. 4, either element 400 or 402, big or little endian processors respectively);

a bus for interconnecting first and second processors (paragraph 0065, lines 1-8 - depicts two different processors as being wired to a data bus).

As for claims 6, 17, and 28, though Makphaibulchoke teaches specifying the location of the data structure, he fails to specifically teach mapping a virtual memory address to a physical one.

Lasserre however teaches mapping a virtual memory address to a physical memory address (paragraph 0060, lines 1-3, each entry in the TLB maps a physical address with every corresponding virtual address).

As for claims 12 and 23, though Makphaibulchoke teaches specifying the location of the data structure, he fails to specifically teach mapping the physical address to a virtual one accessible by a processor.

Lasserre however teaches the entry as mapping the physical address at which the portion of data is stored to a virtual address accessible by a processor (paragraph 0060, lines 1-3, each entry in the TLB maps a physical address with every corresponding virtual address. The processor is able to access the addresses via the TLB as further described in paragraph 0029, line 1 through paragraph 30, line 8 – The TLB contains entries for virtual-to-physical address translation which is accessible by the MMU containing the processor core/s).

As for claims 32, 33, 37 and 38, though Makphaibulchoke teaches a processor, he fails to specific if it strictly for little or big endian data format processing.

Lasserre however teaches a big endian processor and a little endian processor (Fig. 4, elements 400 and 402 respectively).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Makphaibulchoke to further include Lasserre's system with MMU descriptor

having a big/little end bit to control the transfer of data between devices into his own system and method for system for pre-processing data in either a big or little endian operating system. By doing so, Makphaibulchoke would be able to exploit the benefit of utilizing more than one processor (including a DSP for example) which could greatly improve the performance of his system as taught by Lasserre in paragraph 0004, all lines.

As for claims 30 and 35, Makphaibulchoke discloses the at least two types of endian conversion as including a data coherent conversion type (paragraph 0024, Makphaibulchoke 's byte-swapping method is akin to Applicant's data coherent conversion).

5. Claims 4, 9, 15, 20, 27, 41, 45, 50 and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Makphaibulchoke (US PG Publication 2003/0014616 A1) (US PG Publication 2003/0014616 A1) as applied to claims 1, 7, 13, 18, 24, 39, 43 and 47 above, and in further view of Ikumi (US Patent 5,630,084).

As for claims 4, 9, 15, 20, 27, 41, 45, 50 and 51 though Makphaibulchoke teaches data coherent (i.e. byte swapping) conversion, he fails to teach his endian conversion as being address coherent. Ikumi however teaches a system for converting data in little endian to big endian and vice versa by reversing two bits of address referencing one word of four words. In his disclosure, Ikumi teaches reversing the bits of the byte address in order to convert data from big-little (and vise versa) endian format (col. 4, lines 9-21 – Also referring to Fig. 6, byte address reversal is disclosed).

Note Ikumi's system of address reversal for endian conversion is the same as the "address coherent conversion" as shown in Table 1, page 3 of Applicant's specification. It would have been obvious to one of ordinary skill in the art at the time of the invention for Makphaibulchoke to utilize Ikumi's system of endian conversion through address conversion, in addition to his byte swapping endian conversion method. By doing so, Makphaibulchoke would be able to exploit the benefits of using an additional form of endian conversion (i.e. address coherent), which overcomes the draw backs of traditional byte swapping (switching) method which severely complicates operational control during processing of the data (Ikumi – col. 2 – lines 38-46). Ikumi further discusses how the address coherent method overcomes drawbacks of the swapping method in col. 2, lines 48-62 of his disclosure (i.e. operational control of the data processing is markedly improved).

It would have been obvious to one of ordinary skill in the art at the time of the invention for the Makphaibulchoke to utilize Ikumi's system of endian conversion through address conversion, in addition to his byte swapping endian conversion method. By doing so, Makphaibulchoke would be able to exploit the benefits of using an additional form of endian conversion (i.e. address coherent), which overcomes the draw backs of traditional byte swapping (switching) method which severely complicates operational control during processing of the data (Ikumi – col. 2 – lines 38-46). Ikumi further discusses how the address coherent method overcomes drawbacks of the swapping method in col. 2, lines 48-62 of his disclosure (i.e. operational control of the data processing is markedly improved).

6. Claims 31 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Makphaibulchoke (US PG Publication 2003/0014616 A1) and Lasserre (US PG Publication 2002/0069339 A1) as applied to claims 29 and 34 above, and in further view of Ikumi (US Patent 5,630,084).

As for claims 31 and 36, the combined teachings of Makphaibulchoke and Lasserre fail to teach endian conversion as being address coherent. Ikumi however teaches a system for converting data in little endian to big endian and vice versa by reversing two bits of address referencing one word of four words. In his disclosure, Ikumi teaches reversing the bits of the byte address in order to convert data from big-little (and vise versa) endian format (col. 4, lines 9-21 – Also referring to Fig. 6, byte address reversal is disclosed). Note Ikumi's system of address reversal for endian conversion is the same as the "address coherent conversion" as shown in Table 1, page 3 of Applicant's specification.

It would have been obvious to one of ordinary skill in the art at the time of the invention for the combined teachings of Makphaibulchoke and Lasserre to utilize Ikumi's system of endian conversion through address conversion, in addition to his byte swapping endian conversion method. By doing so, the combined teachings of Makphaibulchoke and Lasserre would be able to exploit the benefits of using an additional form of endian conversion (i.e. address coherent), which overcomes the draw backs of traditional byte swapping (switching) method which severely complicates operational control during processing of the data (Ikumi – col. 2 – lines 38-46). Ikumi further discusses how the address coherent method overcomes drawbacks of the

swapping method in col. 2, lines 48-62 of his disclosure (i.e. operational control of the data processing is markedly improved).

Response to Arguments

7. Applicant's amendments and arguments filed have been fully considered, but they are not persuasive.

As for claim 1, Applicant amended the claim to recite the memory management table as "specifying one of the at least two types of endian conversion". Applicant asserts that Makphaibulchoke in fact fails to teach this limitation. Examiner however maintains that Makphaibulchoke does in fact anticipate this limitation for the reasons set forth in the rejection *supra*, and the discussion of Applicant's remarks with respect to claim 24, *infra*. Note the conversion results in writing the converted data structure to the data which "specifies" the type of conversions that were previously determined (i.e. the converted data is now either byte-swapped or bit reversed), therefore the format of the data itself written specify what type of conversion occurred.

As for claim 24, Applicant asserts, "Makphaibulchoke did not to disclose or would not have made obvious writing an entry specifying one of at least two types of endian conversion." Continuing, Applicant contends, "[f]urther, Makphaibulchoke's bit field is not (as the examiner contends) "a single bit which specifies in (sic) byte swapping or bit reversal is appropriate for the data structure." Makphaibulchoke's bit field is an example of a data structure that may be contained in an ACPI table...Therefore, Makphaibulchoke discloses using a bit reversal module to reverse the bits in a bit field

data structure, but does not disclose that a bit field itself specifies if byte swapping or bit reversal is appropriate for a data structure."

This argument however is not persuasive. Examiner maintains, that claim 24 recites, *inter alia*, "one or more table entries having ... a second field for defining a type determined from at least two types of endian conversion." Makphaibulchoke clearly discloses multiple ACPI tables (preferred embodiment describes ten), which include multiple data structures containing data stored in little endian format (paragraph 0024, lines 15-41). These data are converted to a first endian type through one of two types of endian conversion (i.e. byte-swapping or bit-reversal) – paragraph 0024, line 35 through paragraph 0025, final line. Referring again to Fig. 6 and paragraph 0025, all lines, the data is either byte-swapped or bit-reversed based exclusively on information contained within these ACPI tables (both the data structures themselves, and their respective headers within the ACPI tables). The size of the data (evaluated at step 650), and the status of the bit field (evaluated at step 630) indicate/specify to the system what type of conversion to be performed. The information stored within these tables may be broadly construed as a "field" as recited by Applicant, since it is well known to a skilled artisan that "fields" define entries to tables. This interpretation is consistent with Examiner's "broadest reasonable interpretation consistent with Applicant's specification", pursuant to MPEP § 2111.

As for claims 39 and 43, Applicant asserts, "Makphaibulchoke does not disclose that a bit field specifies if byte swapping or bit reversal is appropriate for a data structure. Therefore, Makphaibulchoke fails to disclose or make obvious "accessing a

table entry... [that] includes a conversion-type indicator" as recited in claim 39. Claim 43 is patentable for at least similar reasons."

This argument however is not persuasive. As stated for the argument with respect to claim 24, *supra*, the information contained within the ACPI tables themselves inform the system which type of conversion is to take place on the data structures stored within the table. Since it is clear from paragraph 0025, all lines of Makphaibulchoke that the fields within these tables dictate the type of conversion, one skill artisan would recognize that the tables comprise the "conversion-type indictor[s]" as recited in these claims, else the system would fail to be able to carry out its intended function of endian conversion.

Applicant's argument that "amended claims 7, 13, 18, 29, 34, and 47 are patentable for at least similar reasons as those described above" is not persuasive, as Examiner maintains the previously asserted rejections of all independent claims as per the rejections and arguments set forth *supra*.

Applicant's argument that "[a]ll of the dependent claims are patentable for at least the reasons for which the claims on which they depend are patentable" is rendered moot, as Examiner maintains the previously asserted rejections of all independent claims as per the rejections and arguments set forth *supra*.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

9. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

11. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung S. Sough can be reached on (571) 272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

12. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Craig E Walter
Examiner
Art Unit 2188

CEW

HYUNG SOUGH
SUPERVISORY PATENT EXAMINER
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